ARTERIS IP

sondrel

Case Study

Shortening Leading-Edge ADAS Design Cycles With FlexNoc To Deliver Customer Success

Customer Overview

Sondrel™ provides turnkey design systems-on-chip (SoCs). The company offers application-specific integrated circuit (ASIC) services from system to sign-off. Sondrel design wins include hundreds of leading-edge products for market leaders in mobile phones, cameras, security, augmented reality/virtual reality (AR/VR) and driver assist systems.

The company offers a five-platform suite of applications, from AI at the edge to powerful adaptive data processing. Two are created explicitly for automotive advanced driver-assistance systems (ADAS).

"I have worked with other NoC technologies and have seen a tension between automation/ease of use and stability/predictability. Small changes can generate a significantly different NoC, which then causes disruption to the floorplan." He added, "Arteris provides automation where needed while supporting access tweaking at a low level of the NoC structure. This minimizes disruption to the rest of the structure and preserves stability."

Ben Fletcher
Director of Engineering
Sondrel Ltd.

Business Challenges

- Deliver highly complex ADAS designs from concept agreement to implementation-ready NoC RTL in 1-2 months.
- Respond to client change requests with demonstrable pro/con feedback within a few days.

Design Challenges

- Shorten design cycle from concept to RTL signoff, converged on performance and floorplan objectives.
- Iterate on architectural optimization with realistic software workloads while modeling network topology and other critical NoC architecture choices.
- Prove that full RTL implementation of the NoC mirrors the high-level model used for architecture tuning.

Arteris Solution

- FlexNoC® interconnect IP, and FlexExplorer

Results

- Delivered implementation-ready RTL based on client concept reducing design time from 4-5 months down to 1-2 months on very advanced ADAS SoC designs.
- Demonstrated ability to work with clients in fast debug cycles while adding safety and security support options.

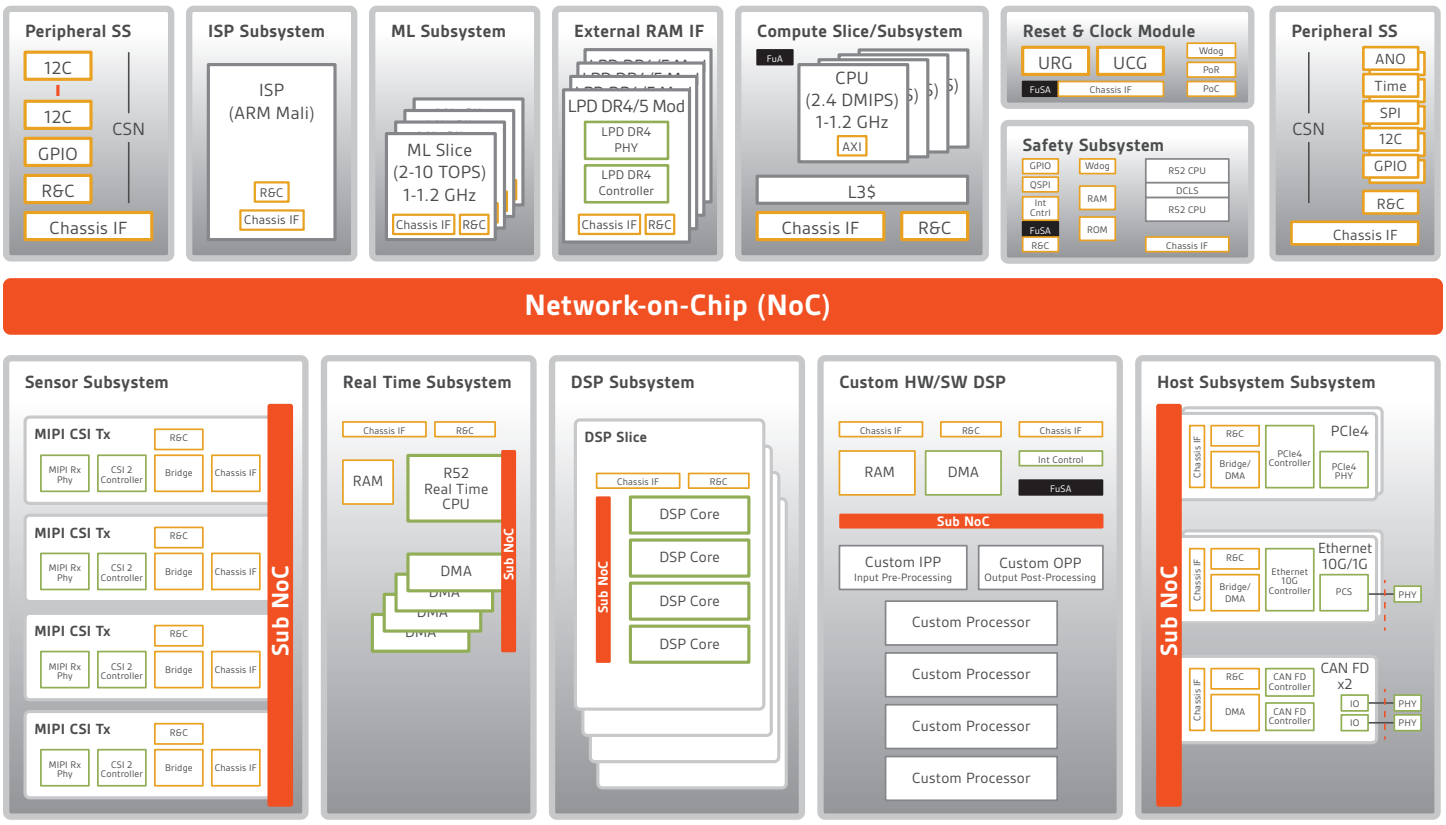

Figure 1. Sondrel SFA 350A Chassis

The Challenge

Sondrel serves a client base whose mission is to build advanced systems automation around complex SoCs. For example, Sondrel has designed its SFA 350A chassis to support autonomous vision ADAS applications. This platform includes a comprehensive range of options for camera shutter control, real-time mobile industry processor interface (MIPI), CV+IMU capture with computational imaging, depth map, point cloud, and simultaneous localization and mapping (SLAM). Additionally, it provides artificial intelligence (AI) inferencing, data fusion such as Kalman filters and Bayesian tracking, and transmission to a command system. All functions can be connected through the subsystems and main network-on-chip (NoC) systems.

Sondrel's customers serve highly competitive markets that require compressed and predictable schedules. Their application-specific chassis platform is a critical component to delivering on this promise. In addition, building on platforms they already understand can improve mapping from concept to high-level implementation.

In a conventional design approach, the architectural planning starts with a spreadsheet view. It then switches to a SystemC model built around the IPs drawn from the SFA platform and a simplified chip network model. NoC modeling based on a generated register-transfer level (RTL) model would follow architectural convergence. This approach has two major drawbacks. First, RTL simulation is too slow to run comprehensive software loads effectively, yet real system performance critically depends on optimizing NoC configuration choices. Second, serializing architecture and NoC design lengthens the project schedule. Sondrel wanted to be able to compress this timeframe significantly by starting NoC configuration and performance optimization while still running software-based testing.

The Solution

Rather than wait for architectural modeling to complete, Sondrel now continues from their first phase exploration with a more accurate SystemC representation. The generic interconnect is replaced with a more realistic architecture view NoC model provided by Arteris' FlexNoC interconnect, enabling them to tune for more accurate performance. This allows them to continue detailed performance tuning against the same software loads used in the prior phase while configuring NoC topology, buffering and other choices to refine their performance and floorplan objectives. Importantly, these are the same configuration choices used in generating the NoC RTL. Starting this analysis in SystemC architecture view with a realistic NoC model, then progressing to RTL with the FlexNoC-generated RTL model, Sondrel can quickly address the challenges. They can run against realistic loads and configure the NoC architecture optimally to meet their client's performance objectives.

As development progresses, Sondrel ultimately switches to a more comprehensive performance verification analysis against the RTL model of the Arteris generated network. This analysis can run on any of the standard simulation platforms. Sondrel adds its own twist by a Python testbench to feed software load traces gathered from the SystemC simulation experiments to drive the RTL performance analysis. Further effort is saved by re-using the software traces from the architecture exploration phase. This process ensures that the tuning accomplished with the SystemC model mirrors in the RTL.

FlexNoC enables stability of NoC generation. Ben Fletcher, Director of Engineering at Sondrel Ltd., noted, "I have worked with other NoC technologies and have seen a tension between automation/ease of use and stability/predictability. Small changes can generate a significantly different NoC, which then causes disruption to the

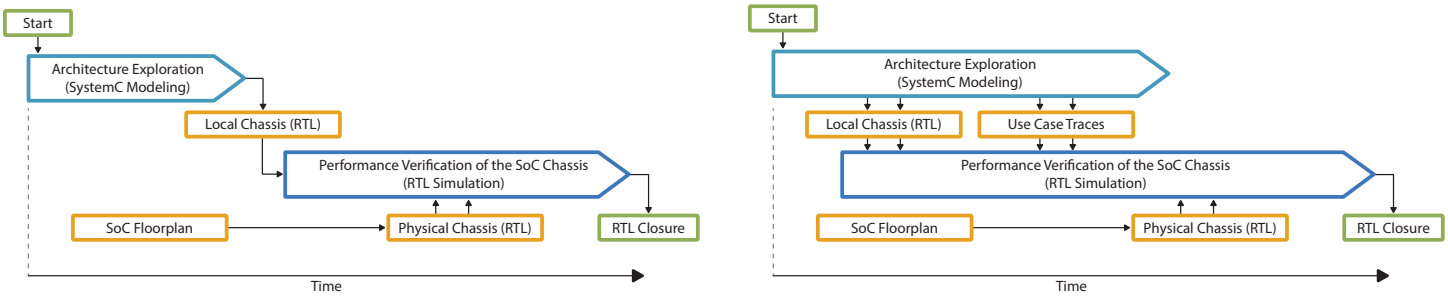

Figure 2. Shifting NoC Performance Verification Left

floorplan." He added, "Arteris provides automation where needed while supporting access tweaking at a low level of the NoC structure. This minimizes disruption to the rest of the structure and preserves stability."

Additionally, Ben stressed that including FlexNoC add-ons offers a solution to avoid getting into a cycle of updates to the NoC design, which can negatively affect the floorplan and leads to further disruption. The company avoids this trap by progressing performance and floorplan enhancements in tandem. FlexNoC add-ons allow them to factor in the need to serialize over long paths through a floorplan to reduce wire count. These choices are then reflected in optimized latencies during performance estimation.

Results

In the past, it would take 4-5 months to reach the point that Sondrel was confident the NoC architecture was solid. By implementing Arteris' FlexNoC, their compressed architecture evaluation cycle can get them to the same spot in 1-2 months. This is an immediate benefit, but there are additional benefits. First, in a concept to silicon engagement, an executable model of the intended design is always more convincing than a paper architecture study. "Our ability to quickly develop a working software model of the SoC, using an accurate SystemC model for the NoC, builds design confidence," according to Ben Fletcher.

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Second, it is common for clients to make late-stage requests for enhancements—adding security support or improving performance bandwidth. Sondrel is able, through their quick cycle development supported by FlexNoC, to turn a proposed model enhancement within a day or two. This reinforces their reputation for providing a premium service—demonstrating expert guidance to help their clients craft the best solutions for their needs.

Summary and Future Plans

Sondrel sees a bright future in customized, complex SoC design services that continue to grow in complexity and rapidly expanding markets and applications. System developers recognize the need for differentiation in silicon to maintain their competitive advantage. Sondrel understands how to manage the complexities of silicon design and optimize for performance and cost. Most of all, the company offers reliability in meeting tight schedules required by customers.

Arteris, a leading provider in system IP, will continue to provide Sondrel with the ability to innovate and support the differentiating features demanded by their customer base. Both companies truly comprehend the challenges and opportunities that advanced SoC design teams face.

About Arteris

Arteris is a leading provider of system IP for the acceleration of system-on-chip (SoC) development across today's electronic systems. Arteris network-on-chip (NoC) interconnect IP and SoC integration technology enable higher product performance with lower power consumption and faster time to market, delivering better SoC economics so its customers can focus on dreaming up what comes next. Learn more at arteris.com.

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