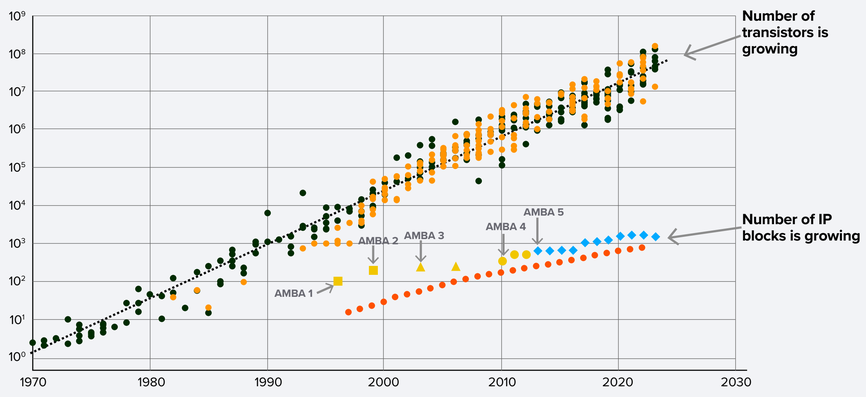
ARTERIS IP

Accelerating Timing Closure for Networks-on-Chip (NoCs) With Physical Awareness

Challenge

Semiconductor Complexity Continues to Grow Exponentially

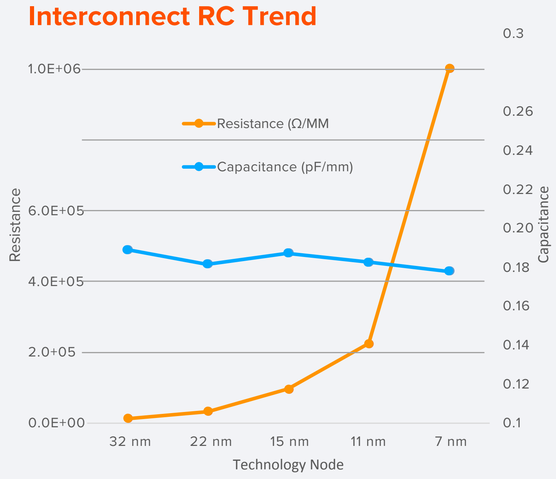


- Complexity of NoC protocols have grown 10x (# of pages)
- Variety of NoC protocols has grown
- NoCs evolve into Super-NoCs when split across chiplets

Physical Implementation is Hard to Predict

- No standard methodology for timing closure for on-chip IP communications
- Process node advances add to RC delays for long, cross-chip distances traveled
- Interconnects that connect different IP blocks span long distances and hence suffer from RC delays

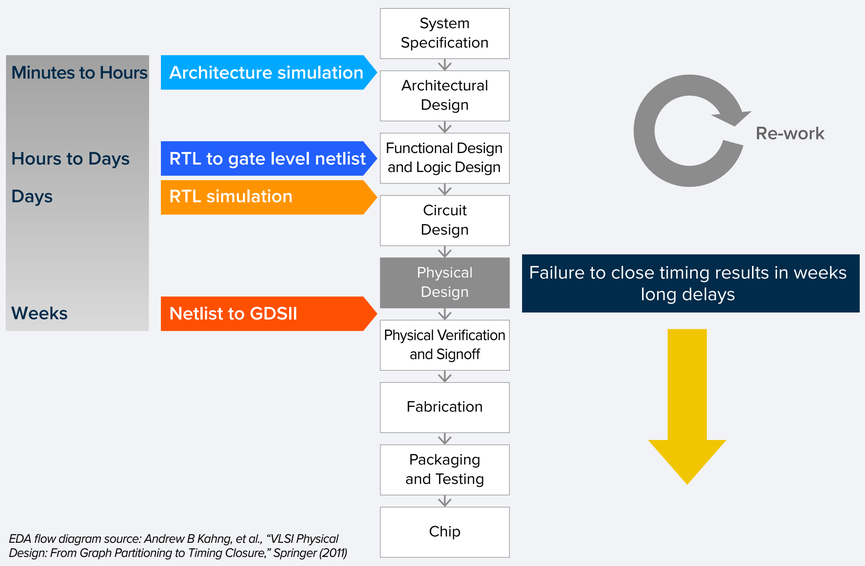
Interconnect RC Trend



Interface-Layer Effects and Grain Scattering Impact Resistance Scaling

Source: Serkan Kincal, et al., "RC Performance Evaluation of Interconnect Architecture Options Beyond the 10-nm Logic Node," IEEE (2014)

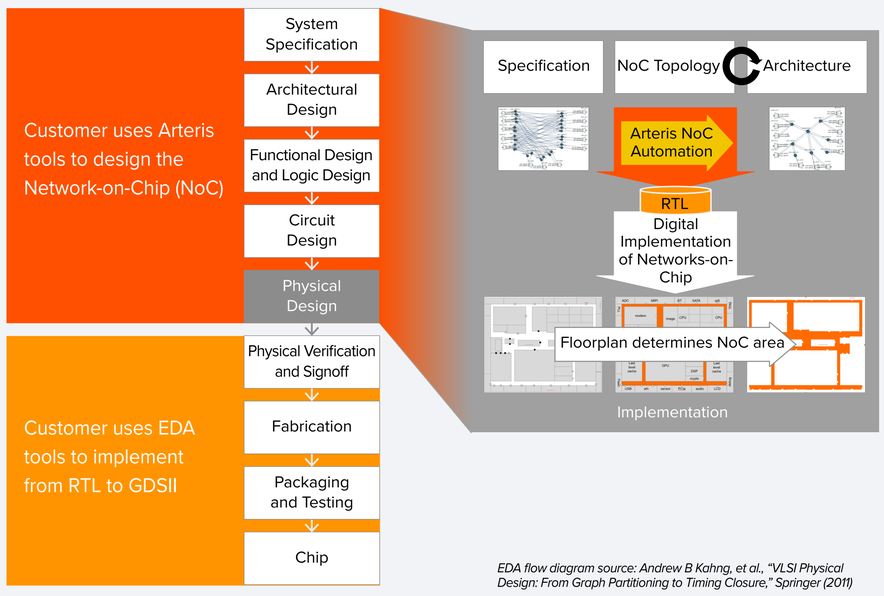
Failure to Close Timing Results in Costly Delays



EDA flow diagram source: Andrew B Kahng, et al., "VLSI Physical Design: From Graph Partitioning to Timing Closure," Springer (2011)

Resolution

Co-Optimized Design Flow Saves Re-work



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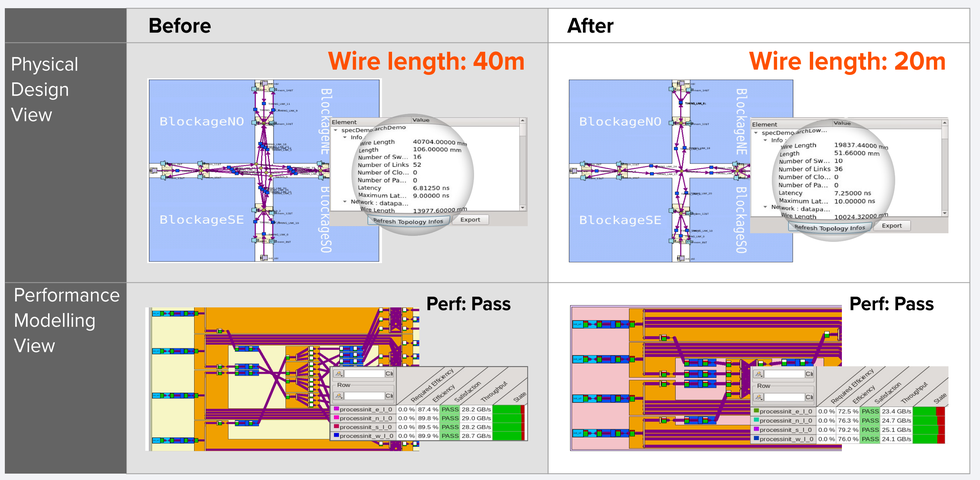
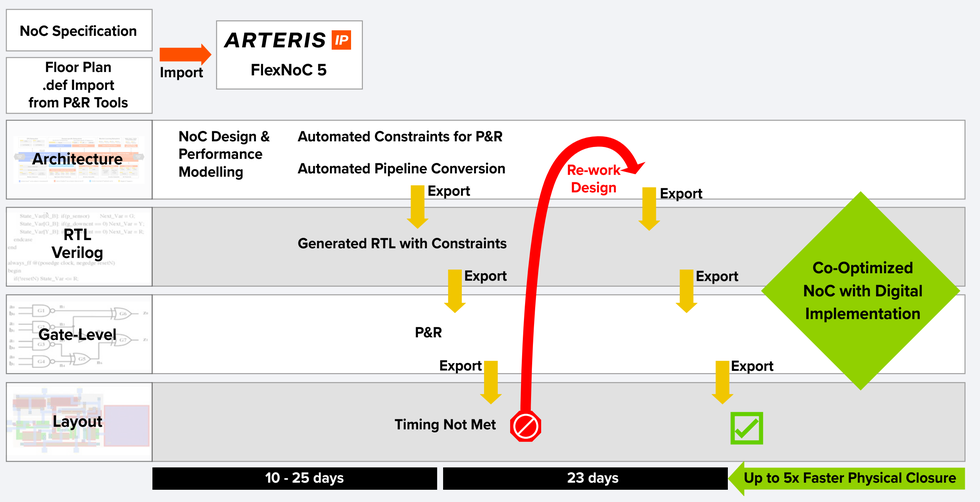
Design Optimization Using Physical + Performance Co-design: 50% Wire Length Reduction Within Performance Goals



Avoiding Late Timing Issues Using Abstraction, Physical Awareness, And Estimation



Highlights

Key Challenge

- The number of IP blocks in systems-on-chip and across chiplets continues to grow.
- The floorplan in digital implementation determines the area that NoCs can consume and with a lack of a standard methodology for timing closure for on-chip IP communications, timing closure in layout often requires a "return to the drawing board" and a re-spin of the NoC architecture.

Key Resolution

- Networks-on-Chip (NoCs) with complex protocols like AMBA AXI, CHI and many others have emerged and continue to grow in complexity.
- Considering the floorplan information during the NoC architecture phase, combined with early estimation of pipeline stages based on .lib technology information and direct connection to digital implementation using constraints, can significantly reduce the time to physical closure.