ARTERIS IP

SCALINX
NEW ART OF SIGNAL CONVERSION

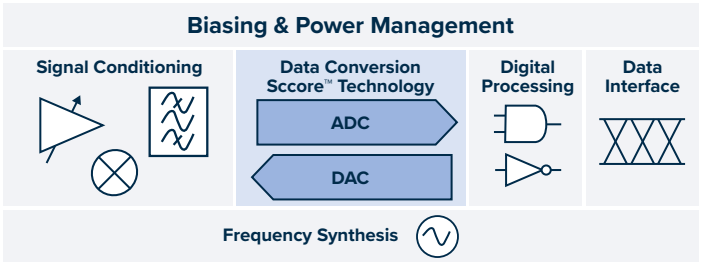
Case Study

Combination of Coherent and Non-Coherent NoCs Facilitates Cutting-Edge SoC Design

Customer Overview

Founded in 2015, and headquartered in Paris, France, SCALINX is a fabless semiconductor company specializing in the design of system-on-chip (SoC) devices.

SCALINX possesses unique expertise in creating cutting-edge SoC solutions in Europe. These designs encompass analog, digital, mixed-signal, and radio frequency (RF) functionality.



The company's SoCs feature best-in-class analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) that combine high speed with superior power efficiency. These data converters enable SCALINX to provide differentiated SoC products for a wide range of markets and applications, including automotive, aerospace and defense, wired and wireless communications, non-terrestrial networks (NTNs), RADAR, and test and measurement (T&M) equipment.

Business Challenges

- Develop a large, next-generation SoC integrating analog, digital, mixed-signal, and RF functionality.

Design Challenges

- Ensure different portions of the design are cache-coherent or non-coherent while maintaining communication and sharing a common address space.
- Support hundreds of IPs employing a wide diversity of interfaces, including APB, AHB, AXI, and ACE.
- Manage tens of physical partitions and hundreds of clock domains.

Arteris Solution

- Ncore® Cache Coherent Interconnect IP.
- FlexNoC® Non-Coherent Interconnect IP.

Results

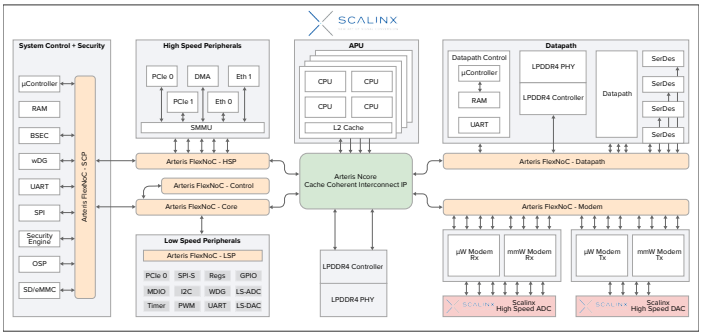
- Completed the bulk of the frontend design in just 1.5 years.

The Challenge

In telecommunications, backhaul refers to the process of transmitting data from smaller, local networks or end-user devices to the core network or central data center. While traditionally achieved through fiber-optic or wired connections, the growing demand for rapid deployment and hard-to-reach areas has accelerated the adoption of wireless backhaul. Currently, the technological enhancements and demands of 5G are pushing the implementation of wireless backhaul to new levels.

While wireless backhaul offers many advantages, it also presents challenges such as power consumption, capacity and bandwidth limitations, latency, reliability, security, and cost. Existing solutions are based on multiple devices mounted on a common printed circuit board (PCB), including central processing units (CPUs), application-specific standard parts (ASSPs), field-programmable gate arrays (FPGAs), ADCs, DACs, and RF chips.

Recently, SCALINX began designing a new SoC targeted at wireless backhaul infrastructure for 5G and 6G networks. This next-generation device leverages SCALINX's unique expertise in combining analog, digital, mixed-signal, and RF functionality on a single SoC.



On the digital side, this new SoC contains multiple digital intellectual property (IP) blocks. These include four processor clusters, each containing four 64-bit high-performance processor cores for a total of 16 processor cores. The SoC also contains two DDR memory controllers, along with many other digital IP functions and peripherals, such as a PCI Express (PCIe) Ethernet modem. In addition to the digital features, analog, mixed-signal, and RF IPs must be considered.

Some of the digital IPs, like the processor clusters and one of the DDR controllers, need to maintain cache coherency, while others do not. This requirement added complexity to the design, especially compared to previous SCALINX SoCs, which were much simpler. These designs involved relatively few IPs, a limited number of clock domains, and a small number of physical partitions.

By comparison, this new SoC design involves hundreds of IPs with multiple hundreds of initiators sourcing data and targets consuming data. Since they come from many sources, these IPs employ a wide diversity of interfaces, including APB, AHB, AXI, and ACE.

Since this new design also involves tens of physical partitions and hundreds of clock domains, the decision was made to use network-on-chip (NoC) interconnect technology. A key requirement was for highly configurable NoC tools that could generate NoC interconnect.

The Solution

"After evaluating various NoC solutions available on the market, it quickly became obvious that Arteris was the leader in this space."

Guillaume Joli
Digital Front-end Lead on Mixed-Signal SoCs
SCALINX

The decision to work with the company was further supported by Laurent Moulin, Digital IC Architect at SCALINX. He was already experienced with Arteris technology from work at a previous company.

In addition to being a proven, trusted solution, one key advantage associated with Arteris NoC technology is that it supports all the standard SoC IP interfaces, including APB, AHB, AXI, ACE, and CHI. This flexibility was significant in addressing the complexity of SCALINX's new SoC design, which required seamless integration of diverse IPs.

For the four processor clusters, these IPs contain Level 1 (L1) and Level 2 (L2) caches. The clusters maintain cache coherence internally but need help maintaining coherence across clusters. Also, all four processor clusters need to maintain cache coherence with one of the SoC's two DDR controllers. The solution here was to use a single Arteris Ncore cache-coherent NoC. This NoC was deployed in a full mesh topology, acting as a common Level 3 (L3) cache to all the IPs.

Regarding the rest of the SoC, which encompasses tens of physical partitions and hundreds of clock domains, it was decided to use a divide-and-conquer approach involving 11 Arteris FlexNoC non-coherent NoCs, all implemented using traditional tree topologies. The SoC's second DDR controller, which is used by the application, is attached to one of these NoCs.

In this design, all the NoCs, both cache-coherent Ncore and non-coherent FlexNoC, are linked by bridges, and all share a common address space.

"I think one of the key aspects to NoC technology from Arteris is the tool's ability to create customized NoCs, to simulate the results, and to quickly iterate between solutions. This allowed us to fine-tune each NoC to our exact needs, thereby providing the best trade-off between power, performance, and area (PPA)."

Guillaume Joli
Digital Front-end Lead on Mixed-Signal SoCs
SCALINX

Also, both Guillaume and Laurent offer enthusiastic praise for the high level of technical support provided by their local Arteris office.

Results and Future Plans

The results have been highly impressive, as the engineers have been working on this SoC design project for only 1.5 years. In that short time, the frontend team has already handed over the register transfer level (RTL) representation of the bulk of the design to the backend physical design team for place and route.

The frontend team continues to fine-tune the observability and security aspects of the device. Meanwhile, both the frontend and backend teams are iterating and tweaking to achieve timing closure.

The SCALINX team recognized the value of the FlexNoC physically aware feature in addressing their design needs. This means these tools can optimize for physical layout constraints such as floorplanning, routing, and wire lengths, thereby achieving better performance, power efficiency, and area utilization.

"Automatic physically-aware NoC generation and pipeline stage insertion dramatically increase the productivity of our designers and the correct-by-construction quality of the final design."

Laurent Moulin
Digital IC Architect
SCALINX

Existing wireless backhaul solutions are based on the combination of multiple devices mounted on a common PCB. By comparison, this new SoC from SCALINX will provide higher performance while consuming a quarter of the power, all at a fraction of the cost.

The plan is to release this new SoC to the market in the following year. At the same time, SCALINX is already planning future generations of devices, all of which will take full advantage of state-of-the-art NoC technology from Arteris.

About Arteris

Arteris is a leading provider of system IP for the acceleration of system-on-chip (SoC) development across today's electronic systems. Arteris network-on-chip (NoC) interconnect IP and SoC integration technology enable higher product performance with lower power consumption and faster time to market, delivering better SoC economics so its customers can focus on dreaming up what comes next. Learn more at arteris.com.

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